Tuning arrangement

The invention relates to a tuning arrangement for receiving a plurality of signal channels and for tuning to a specific of said plurality of signal channels, the arrangement comprising a polyphase mixer for mixing said specific signal channel to an intermediate frequency which is lower than twice the bandwidth of the channel, a polyphase IF filter for rejecting the negative frequencies in the mixer output signal and a polyphase group delay equalizer connected to the output of the polyphase IF filter. Such a tuning arrangement, which is proposed in figure 6 of applicant's prior European patent application EP 01201757.0, has the advantage that the tuning arrangement can be implemented with a high degree of monolithic integration without many discrete components and without the costs involved in adjusting such discrete components.

In most applications of a tuning arrangement of the above kind the group delay has to be kept within certain limits. For instance, in analogue TV a delay results in a horizontal shift in the picture and one pixel shift approximately corresponds with a delay of 80 ns. Therefore it is necessary that the variations in the group delay be kept below 80 ns. This is why the above-described tuning arrangement is equipped with a group delay equalizer.

Usually, prior art group delay equalizers have an all pass transfer function with pole-zero pairs which lie symmetrically with respect to the real axis of the complex frequency plane, with the poles and zeros of the pairs lying symmetrically with respect to the imaginary axis of that plane, whereby the poles are located in the left half of the plane and the zeros in the right half. With other words, with a group delay equalizer with two pole-zero pairs, the two poles are located at $p = -\sigma \pm j\omega_s$ and the two zeros are located at $p = \sigma \pm j\omega_s$ where ω_s represents the shift along the imaginary axis and σ the shift along the real axis.

The present invention makes use of the fact that in case of a group delay

equalizer for a low IF tuning arrangement a substantial improvement can be obtained when in accordance with the invention the tuning arrangement is characterized in that the transfer function of the group delay equalizer has, for the frequency range of interest, only one or more pole-zero pairs alongside of the positive imaginary axis of the complex frequency plane with the pole(s) and the zero(s) of said one or more pairs lying substantially symmetrically with respect to said positive imaginary axis. Therefore according to the invention, in case the equalizer has only one pole-zero pair, the pole lies at $-\sigma + j\omega_s$ and the zero at $\sigma + j\omega_s$.

The invention is based on the following recognition: At the lower frequencies the group delay of the low IF filter is high and decreases with increasing frequency. The equalizer group delay originating from the pole-zero pair(s) in the upper half of the complex frequency plane increases with increasing frequency and is therefore able to at least partly correct or equalize the group delay variations of the IF filter. However, the group delay originating from the pole-zero pair(s) in the lower half of the complex frequency plane decreases with increasing frequency. Therefore such pole-zero pair(s) is not only useless for the equalization process but even counteracts this process. Consequently, it is better to avoid any pole-zero pair in the lower half of the complex frequency plane, what is very well possible with a polyphase group delay equalizer.

A preferred embodiment of a group delay equalizer for use in a tuning arrangement according to the invention is characterized in that said polyphase group delay equalizer comprises an in phase part and a quadrature phase part, each of said parts comprising a balanced operational amplifier, first conductances and first capacitances connected in parallel between each output and the inverting input of the operational amplifier for constituting the pole in the complex frequency plane, second conductances between each input of the part and one of the inputs of the operational amplifier and second capacitances between each input of the part and the other of the inputs of the operational amplifier for constituting the zero in the complex frequency plane and further conductances connecting the inputs of the operational amplifier of each part to the inputs and to the outputs of the other of said parts for shifting the pole and the zero along the positive imaginary axis of the complex frequency plane. In case the amplitude of the transfer function is equal to unity, the said first and second

capacitances are equal, the said first and second conductances are equal and said further conductances are equal. Compared with conventional group delay equalizers the advantages of this kind of group delay equalizers are: less noise contribution, less power consumption and less chip-area or better performance with unchanged chip area. Moreover this kind of group delay equalizers is easy to design. The group delay curve as a function of the frequency is a symmetrical "hill" with the shape of the "hill" being determined by said first and second conductances and the position of the "hill" being determined by said further conductances.

In some cases the group delay to be equalized may be corrected by a group delay equalizer having only one pole-zero pair in the upper half of the complex frequency plane. In case the group delay to be equalized is larger or more complicated this group delay may be equalized by an equalizer having two or three pole-zero pairs in the upper half of the complex frequency plane. However, in accordance with another aspect of the invention, a tuning arrangement having such larger or more complicated group delay to be equalized may preferably be characterized in that a cascade of group delay equalizers is connected to the output of the polyphase IF filter, each of said group delay equalizers having only one pole-zero pair alongside of the positive imaginary axis of the complex frequency plane.

The invention will now be described with reference to the accompanying drawings. Herein shows

Fig. 1 a block schematic diagram of a tuning arrangement according to the invention,

Fig. 2a detailed schematic diagram of the group delay equalizer for use in the tuning arrangement of figure 1,

Fig. 3 a pole-zero diagram of the transfer function of the group delay equalizer as depicted in figure 2 and

Fig. 4 graphs showing the course of the group delay as a function of the frequency of different parts of the arrangement of figure 1.

The arrangement of figure 1 is primarily intended for the reception of cable- TV-signals. The arrangement comprises an RF band pass filter 1 which is preferably constituted by a bank of fixed tuned filters, each of which can be switched into operation by a switching signal that is dependent on the local oscillator tuning. Because the mixing process, to be described hereafter, is performed by multiplying the RF-signal with a symmetrical local oscillator square wave that comprises the uneven harmonics of the local oscillator frequency, it is the primary purpose of the RF band pass filter to suppress the 5^{th} harmonic of the RF-signal by about 50 dB. Suppression of the 3^{rd} harmonic is not necessary because the mixing product of the RF 3^{rd} harmonic and the local oscillator 3^{rd} harmonic is cancelled in the polyphase mixer.

In an RF polyphase filter 2 the output of the RF band pass filter 1 is converted into a polyphase RF signal whose negative frequencies are suppressed and this polyphase RF signal is subsequently mixed with a polyphase balanced local oscillator signal from a frequency synthesizer 4 in a full polyphase mixer 3. In the mixer 3 the selected channel is converted to a low IF TV-signal of e.g. 1,5 to 6,4 MHz with the picture carrier at 5,7 MHz.

An IF polyphase filter 5 realizes the larger part of the channel selectivity and moreover suppresses the negative frequencies between -8 and -1 MHz to about -60 dB. The IF output of this filter is applied, through a polyphase group delay equalizer 6 to be described hereafter, to an anti aliasing filter 7 whose primary purpose is to suppress the undesired higher frequencies (> 8 MHz) that would otherwise give rise to aliasing distortion in the AD-converter to follow (not shown). From the anti aliasing filter 7 non-polyphase signals are outputted.

The polyphase group delay equalizer of figure 2 comprises two identical parts R and R'. The part R has input terminals I_1 and I_2 receiving an input signal V_1 to be equalized and output terminals O_1 and O_2 delivering the equalized output signal V_2. The part R' receives at its input terminals I'_1 and I'_2 the same but 90° phase shifted input signal jV_1 and delivers at its output terminals O'_1 and O'_2 the 90° phase shifted output signal jV_2. The elements of the part R' are indicated by the same reference numerals as those of part R except that they are provided with an accent.

The part R comprises a balanced operational amplifier A. The output terminals of the amplifier are each connected through a parallel arrangement of a conductance G_1, G_2 and a capacitance C_1, C_2 to the respective inverting input N_1, N_2 of the operational amplifier. The input terminals I_1 and I_2 are connected through conductances G_3, G_4 to the amplifier inputs N_1, N_2 respectively. Moreover these input terminals are cross-connected through capacitances C_4, C_3 to the amplifier inputs N_2, N_1 respectively.

The conductances G_1 and G_2 have equal values and the same applies to the capacitances C_1 and C_2. The parallel arrangements G_1-C_1 and G_2-C_2 generate a pole P in the complex frequency plane representing the transfer function V_2/V_1 (see figure 3). In this plane the quotient $G_1/C_1 = G_2/C_2 = \sigma$ is the distance of the pole to the imaginary axis. Similarly the conductances G_3 and G_4 have equal values and the capacitances C_3 and C_4 have equal values. The arrangements G_3-C_3 and G_4-C_4 generate a zero Z in the complex frequency plane of V_2/V_1 (see figure 3), however, because of the cross connection of the two capacitances, this zero lies at the right hand side of the imaginary axis while the pole lies at the left hand side of this axis. The quotient $G_3/C_3 = G_4/C_4$ determines the distance of the zero to the imaginary axis. For the equalizer to have a uniform amplitude characteristic (all pass) it is necessary that the pole and the zero lie symmetrically with respect to the imaginary axis and this requirement implies that $G_1/C_1 = G_2/C_2 = G_3/C_3 = G_4/C_4 = \sigma$. The amplitude (gain) of the group delay equalizer equals unity when all four conductances have equal values G and all four capacitances have equal values C whereby the quotient $G/C = \sigma$ determines the distance of the pole and the zero to the imaginary axis.

The arrangement described so far is not able to perform the required equalization, This is because the pole and the zero then both lie on the real axis of the complex frequency plane with the result that the group delay is largest at zero frequency and decreases with increasing frequency, while also the group delay to be equalized is maximal at zero frequency. Therefore the arrangement of figure 2 further comprises four conductances H_1, H_2, H_3 and H_4 which are connected respectively between the amplifier input N_1 and the part R' output O'_2, the amplifier input N_2 and the part R' output O'_1, the amplifier input N_1 and the part R' input I'_1 and between the amplifier

input N_2 and the part R' input I'_2. The conductances H_1 and H_2 are equal and cause extra currents flowing to the amplifier inputs N1 and N2 respectively and these extra currents cause a shift of the pole P along the positive imaginary axis over a distance $H_1/C_1 = H_2/C_2$. Also the conductances H_3 and H_4 are equal and cause extra currents flowing to the amplifier inputs N1 and N2 respectively. These cause a shift of the zero Z along the positive imaginary axis of the plane over a distance $H_3/C_3 = H_4/C_4$. For the equalizer to retain its all pass character these shifts have to be equal so that $H_1/C_1 = H_2/C_2 = H_3/C_3 = H_4/C_4 = \omega_s$ (see figure 3). Of course when all four capacitances are equal also all four conductances have to be equal and the shift $\omega_s = H/C$.

Figure 4 shows the result of the group delay equalizing by means of the equalizer constructed and dimensioned as described with reference to figures 1, 2 and 3. Curve I shows the group delay of the polyphase IF filter 5 as function of the frequency. The group delay equalizer 6 not only equalizes the group delay of the IF filter 5 but also of the anti aliasing filter 7. Therefore curve II of figure 4 depicts the total group delay of the two units 5 and 7. Vertical stroke lines indicate the limits of the frequency range of the low IF TV signal to be handled. It can be seen from curve II that the group delay of the two units varies between 130 and 290 ns.

Curve III of figure 4 shows the group delay of the polyphase group delay equalizer 6. This curve is a symmetrical "hill" with a top of 170 ns at 5,4 MHz. It may be noted that, with given capacitances, the shape of the "hill" is determined only by σ i.e. by the G-conductances of the equalizer and that the position of the "hill" is determined only by ω_s i.e. by the H-conductances of the equalizer.

Curve IV of figure 4 shows the total equalized delay that is the sum of the curves II and III. This delay ranges from 325 ns at 1,5 MHz till 250 ns at 3 MHz, i.e. the delay variation is 75 ns, which is within the limit of 80 ns set before.

As has already been mentioned in the preamble, more than one group delay equalizer can be connected in cascade so that the group delay of the individual equalizers is added. The individual equalizers may have the same or different pole-zero patterns.